

ABSTRACT

A data latch system includes a data input for providing a first data bit having a first duration and a second data bit having a second duration, and a data output for providing the first data bit for the first and second durations. First sampling circuitry is connected to the data input and the data output for the first duration to provide the first data bit to the data output. Second sampling circuitry is connected to the data input and the data output for the second duration to provide the second data bit inverted to the data output. Holding circuitry connected to the data output for the second duration holds the first data bit and the second sampling circuitry connects the second data bit inverted to the data output to enhance the held first data bit when the first and second data bits have different states.

10051836-011602